Name	**Mark John Butcher** **BSC (Hons), MPhil, MIEE**

Born	25.10.1963 Bromsgrove, England
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Education	*1977-82* South Bromsgrove High School *1982-86* Polytechnic of Wales (University of Glamorgan)
Qualifications	**1986: First Class Honours** Degree in Electrical and Electronic Engineering. Final year project: "Simulation of the HC6303 MCU using the Hilo-3 simulation package." **1991: MPHIL** "Radio Frequency Circuit Design for Surface Mounted Production Assemblies." 1991 in collaboration with Autophon UK and the Polytechnic of Wales.
Languages	English- mother tongue German- written and spoken fluency French- good working knowledge
Sports	Mountain bike, golf, hiking
Hobbies	Classic automobiles, software development techniques
Present situation	Since 1995 – director of M.J.Butcher Consulting
Websites	www.mjbc.ch / www.uTasker.com

Detailed Employment History:

Jan. '85- Aug '85   Department of Bio-Engineering Research Unit,
University Hospital of Wales, Cardiff, CF4 4XW.
Supervisor: Dr. Ken McKarthy.

Research work concerning ultra-sonic measurements with a PVDF hydrophone. Work involved designing low-noise, wide-band amplifiers for the purpose (100kHz-40MHz). Video signal processing was also experienced due to the recording and calibration of the output from ultra-sound scanners. Designed phase lock circuitry to synchronise such video images to the BBC microcomputer.

Aug. '86- Jun. '89   **Autophon (UK) Ltd**., Cypress Drive, St. Mellons, Cardiff.
Supervisor: Mike Wild MPhil.

Design of radio circuitry for cordless telephones (47MHz and 1.7MHz). Initially worked on the final stages of the "Solo" cordless telephone and then designed the "Piccolo A" cordless telephone and was responsible for its approval to BABT (British Approvals Board for Telecommunications) and DTI MPT 1322 radio specifications. Became "Product Responsible Engineer" for the "Piccolo B" and designed handset hardware (Narrowband FM and companding circuitry).

Jul. '89- Sep. '91   **Ascom Radiocom AG**., Weissensteinstrasse, 81,
4503 Solothurn, Switzerland.
Supervisor: Alan Sahuc. Project leader of project ASTREE.

Software engineering on SNCF (French National Railways) track to train radio project. Developed a low frequency signalisation channel and the system software drivers (M8274 and D72001 in ASYNC, COP and BOP (HDLC)).

From July 1990 was responsible for software and hardware of an embedded project (ASTREE – automatic, real-time train tracking system) which also demanded the supervision of the development of new modem and processor modules. The sub-system allows the tracking of trains and the transmission of data between supervisory computers in the trains and along the rails, while respecting the overall system's functionality. A test system was installed in mid- 1992 in Paris and consisted of 19 base stations and 100 mobile units.

Software was written in 'C' and assembler, operating in the Whitesmith's "C-Executive" real time environment. Intel 80186 microprocessors were utilised for general processing functions.

Sep. '91 - Apr. '93   Group leader of "Bahnfunk" hardware section.
Reporting to Ben Wahlström. Development leader.

Responsible for 7 hardware engineers during the fabrication introduction of the SNCF track-to-train system: fix station, mobile station, railway station, frontend station and dispatch centre. This involved factory support, supplying the final fabrication, customer, installation and test documentation.

From April 1992 became responsible for the redesign of the track-to-train HW/SW concept with the goal of reducing product costs to 40% in order to maintain present market and to be competitive in new markets. Budget was 1.4 MsFr and time scale 12 months to the first product; a compatible fix station.

The resulting architecture was based on the Motorola 68302 communication processor (optional slave processor for multiple modem requirements) with a 56156 DSP performing hardware functions, communicating over a shared 16 bit Motorola bus with arbitration. The original network software was transferred to the Motorola environment and the resulting fix station product consists of 4 "ICS-2" extended Eurocards in place of 28 older variants. Analogue buses were replaced by PCM buses.

Apr. 93 - Feb. 95   Technical Project Leader of a multi-national railway radio system project: **Ascom Radiocom AG**., CH-5506 Mägenwil
Reporting to Alan Sahuc (Product manager) and Philipp Thalmann (Project manager).

Ascom Radiocom AG was successful in winning a prestigious track-to-train contract based on the ICS-2 HW/SW concept: PBKA (Paris, Brussels, Köln, Amsterdam) for high speed trains (TGV-Q) – later known as the Thalys (http://www.thalys.com/). The goal was the design and delivery of a mobile unit (with operating console) which is compatible with the present infra-structures in France, Belgium, Holland and Germany. The post involved the direct technical responsibility for 5 HW engineers and 6 SW engineers.

Prototypes were delivered in October 1994 and the first level of acceptance was obtained in December 1994. The first Thalys services started between Paris and Brussels on 4th June 1996 and the entire network has been in commercial operation since the end of 1999 - http://en.wikipedia.org/wiki/Thalys .

Feb. 95 – present   Director of **M.J.Butcher Consulting**

M.J.Butcher Consulting offers HW and SW design and consulting services involving the design of analogue and digital circuits, layout and production support as well as embedded software development for DSP and embedded processors.

Since 2005 the company has been offering the µTasker operating system with TCP/IP stack and simulator for a range of single-chip processors. The project concentrates on increasing efficiency in projects based on single-chip processors, whereby optimal use of available processor resources and development acceleration based on simulation techniques are the focus.

The µTasker project – www.uTasker.com - is a result of practical experiences from over 10 years of customer developments and has gained recognition from various semi-conductor manufacturers who also include the µTasker solution in their portfolio of 3rd party tools – *Freescale, ATMEL, Texas Instruments (Stellaris).*

Freescale Design Alliance Member since 2006 and Freescale Connect Partner since 2014:

"The Freescale Connect Partner Program is your essential source for embedded designs based on Freescale solutions. The program comprises a global network of independent engineering companies that offer the vital tools, software, technology, engineering services and training to speed your design.
From reference boards to optimized software, Freescale Connect provides a powerful and comprehensive ecosystem that partners with you in making the world a smarter, more connected place."

More recent extensions include USB stack, FAT file system, CAN, graphics library, protocol extension packages and an increasing number of supported single-chip processors. The project has over 2'000 registered users who are intensively supported in the µTasker forum http://www.uTasker.com/forum/ and has been used commercially in around 200 projects in more than 20 countries.

Present focus is on the Freescale Kinetis family of Cortex M4 processors and supporting companies with their embedded system designs and project developments.

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